Claims

1. A communication system comprising:

a first printed circuit board;

a conductive path affixed to the printed circuit board;

a driver circuit affixed to the first printed circuit board and coupled to the conductive path to output onto the conductive path a signal having a voltage level that varies in time between at least three distinct levels representative of at least three distinct digital values, the driver circuit including an equalization circuit to adjust the voltage level of the signal output by the driver circuit at a first time according to a digital value represented by the signal at a previous time; and

a receiver circuit affixed to the first printed circuit board and coupled to receive the signal from the conductive path to determine which of the at least three distinct digital values is represented by the signal at a given time.

2. The system of claim 1, wherein the driver and receiver circuits are respective integrated circuits affixed to the first printed circuit board.

3. The system of claim 1, wherein the driver and receiver circuits and conductive path are incorporated within a common integrated circuit that is affixed to the first printed circuit board.

4. The system of claim 1, wherein at least one of the driver and receiver circuits is coupled to a second printed circuit board that is affixed to the first printed circuit board.

5. The system of claim 4, wherein the second printed circuit board is removably affixed to the first printed circuit board.

6. The system of claim 1, wherein the driver circuit receives a plurality of input signals, and the equalization circuit receives and delays said plurality of input signals.

7. The system of claim 1, wherein the driver circuit receives a plurality of input signals, and the equalization circuit receives and inverts said plurality of input signals.

8. The system of claim 1, wherein the equalization circuit compensates for attenuation of the signal in the conductive path.

9. The system of claim 1, wherein the equalization circuit compensates for reflection of the signal in the conductive path.

10. The system of claim 1, wherein the equalization circuit compensates for crosstalk generated by the signal in a second conductive path.

11. The system of claim 1, wherein said signal has a fourth voltage level that varies in time between at least three distinct levels, the fourth level representative of a fourth digital value that is distinct from the at least three distinct digital values.

12. A communication system comprising:

a signaling device configured to produce a set of N signal levels representing a set of logical states, said device including a main driver adapted to receive a plurality of input signals and to output a signal, based on said input signals, that shifts over time between said signal levels; and

an equalization mechanism containing an auxiliary driver that is substantially proportional to said main driver, said equalization mechanism adapted to receive said input signals and generate a set of N equalization signals based on said input signals, wherein N is greater than two.

13. The system of claim 12, wherein for each of said signal levels, an activation level of said main driver and an activation level of said auxiliary driver sum to equal N.

14. The system of claim 12, wherein said equalization mechanism includes an element adapted to invert said input signals.

15. The system of claim 12, wherein said equalization mechanism includes an element adapted to delay said input signals by a time substantially equal to a bit period.

16. The system of claim 12, wherein said main driver and said auxiliary driver each include a current source, and said signal levels are voltages that are in a range between ground and a positive voltage.

17. The system of claim 12, wherein said equalization mechanism is configured to compensate for attenuation of said signal over a signal line.

18. The system of claim 12, wherein said equalization mechanism is configured to compensate for reflection of said signal over a signal line.

19. The system of claim 12, wherein said signal is transmitted over a first signal line and creates crosstalk in a second signal line, and said equalization mechanism is coupled between said first and second lines and configured to compensate for said crosstalk in said second line.

20. A communication system comprising:

a first main driver adapted to receive a first plurality of input signals and to output on a first line a first signal that varies over time between N output levels based on said first plurality of input signals, and a second main driver adapted to receive a second plurality of input signals and to output on a second line a second signal that varies over time between N output levels based on said second plurality of input signals, said main drivers adapted to shift from a first of said signal levels to a second of said signal levels by a transition having N-1 possible values for each said first signal level, said transition being substantially equal to a multiple of a difference between adjacent signal levels, said signal levels representing a set of logical states; and

a first equalization mechanism including a first auxiliary driver having a gain that is substantially proportional to and smaller than said first main driver, said first equalization mechanism configured to receive said first plurality of input signals and to output on said second line a third signal, whereby said third signal compensates for crosstalk on said second line generated by said first signal.

21. The system of claim 20, wherein said main drivers and equalization mechanism each include a current source, and said signal levels are voltages that are in a range between ground and a positive voltage.

22. The system of claim 20, wherein said equalization mechanism further comprises a delay element and a second auxiliary driver having a gain that is substantially proportional to and smaller than said first main driver, said second auxiliary driver configured to receive said first plurality of input signals after delay by said delay element, and to output on said first line a fourth signal.

23. The system of claim 20, wherein said equalization mechanism further comprises an inversion element and a second auxiliary driver having a gain that is substantially proportional to and smaller than said first main driver, said second auxiliary driver configured to receive said first plurality of input signals after inversion by said inversion element, and to output on said first line a fourth signal.